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PATENT  
8040-1022

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re application of:

Hirotaka NAKANO et al.

Confirmation No. 9420

Serial No. 09/855,723

GROUP 2825

Filed May 16, 2001

Examiner Magid Y. Dimyan

SYSTEM OF MANUFACTURING SEMICONDUCTOR  
INTEGRATED CIRCUIT

AMENDMENT AFTER FINAL REJECTION

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

July 7, 2004

Sir:

Responsive to the Official Action of April 16, 2004,  
please amend the above-identified application as follows:

**Amendments to the Specification** begin on page 2 of this  
paper.

**Amendments to the Claims** are reflected in the listing  
of claims that begins on page 4 of this paper.

**Remarks** begin on page 15 of this paper.

An **Appendix** is attached which follows the signature page  
of this paper.